Comparative study of Complementary Metal Oxide Semiconductor (CMOS) and Dynamic Threshold Metal Oxide Semiconductor (DTMOS) logic gates

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ABSTRACT

In demand of green technology required a device that consume less power to operate at minimum cost and long operating time. Currently CMOS is the major component on Integrated Circuit (IC) with DTMOS as a new innovation that can rival its domination. This paper showed comparison between CMOS and DTMOS logic gates by using Mentor Graphic simulation of silicon at 0.13µ size. The parameters used are propagation delay, maximum operating frequency and power dissipation of the transistor. The CMOS and DTMOS research is always about the power consumption properties. However, DTMOS has low power consumption to win over CMOS but lack of stability in term of maximum operating frequency and propagation delay. On top of that, a combination of CMOS and DTMOS logic gates was possible under certain circumstances.

Keywords: Maximum operating frequency; propagation delay; power dissipation

ABSTRAK

Dalam memenuhi tuntutan teknologi hijau memerlukan alat peranti menggunakan kuasa yang kecil untuk beroperasi pada kos minimum dan jangka masa operasi yang panjang. Pada masa kini CMOS adalah komponen utama dalam pembuatan litar bersepadu (IC) dengan DTMOS sebagai inovasi baharu yang boleh menyaingi dominasinya. Jurnal ini menunjukkan perbandingan diantara logik get CMOS dan DTMOS dengan menggunakan simulasi Mentor Graphic pada silicon bersaiz 0.13µ. Parameter yang digunakan adalah lengah rambatan, operasi maksimum frekuensi dan pelesapan kuasa bagi transistor. Penyelidikan CMOS dan DTMOS selalu berkaitan dengan penggunaan kuasa. Walau bagaimanapun, DTMOS mempunyai penggunaan kuasa rendah mengatasi CMOS tetapi kurang kestabilan bagi operasi maksimum frekuensi dan lengah rambatan. Tambahan pula, combinasi logik get CMOS dan DTMOS adalah tidak mustahil dibawah keadaan tertentu.

Kata Kunci: Operasi maksimum frekuensi; lengah rambatan; pelesapan kuasa

INTRODUCTION

Digital device is a must nowdays, with user always hoping for better performance in term of long life battery span, large memory capacity and high resolution display. Submicron technology allow integrated circuit (IC) to have smaller transistors, make a device to have higher processing power at a pack and small size. Designer had successfully made an IC at a small scale factor but the big power dissipation still concern as a main issue. Low usage power means that lowering the power dissipation and one way to do that is by supplying low voltage to the IC. Moreover, the less voltage that being used on IC can make a device to operate using more small and light weight battery (Mustapa et al. 2008). Because of that designer used CMOS to overcome this problem.

CMOS is a technology that being used on many IC design. CMOS circuits used a combination of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) from pMOS and nMOS types to operate logic operation. The CMOS transistors can only operate when $V_{gs} > V_{th}$ and $V_{ds} \geq V_{gs} - V_{th,}$ on saturated region. To produce a nano scale transistors was an advancement of today technologies. However, there was a limitation for CMOS transistors to operate in this scale. For example when the voltage supplied is less than 1V, it is hard to control current from drain to source without adding the gate voltage (V_g). Size scaling under 36nm on new technology make the saturation region become narrow. This lead to the short channel effect on logic gates becoming significantly high. Thus, the scaling method for MOSFET is a dead end.

This problem can be solve by using DTMOS technique in conventional transistors. The DTMOS is a solution in fabricate IC at where the logic gates can operate with less power dissipation compared to CMOS logic gates (Andrade, 2012). The foundation of DTMOS technology is the ability of the threshold voltage (V_{th}) to operate at very low voltage but still give performance equivalent to CMOS (Vincence et al. 2002). This journal is about comparison of CMOS and DTMOS in term of power dissipation, maximum operating frequency and propagation delay on basic logic gates of NAND, NOR, and inverter.

METHODOLOGY

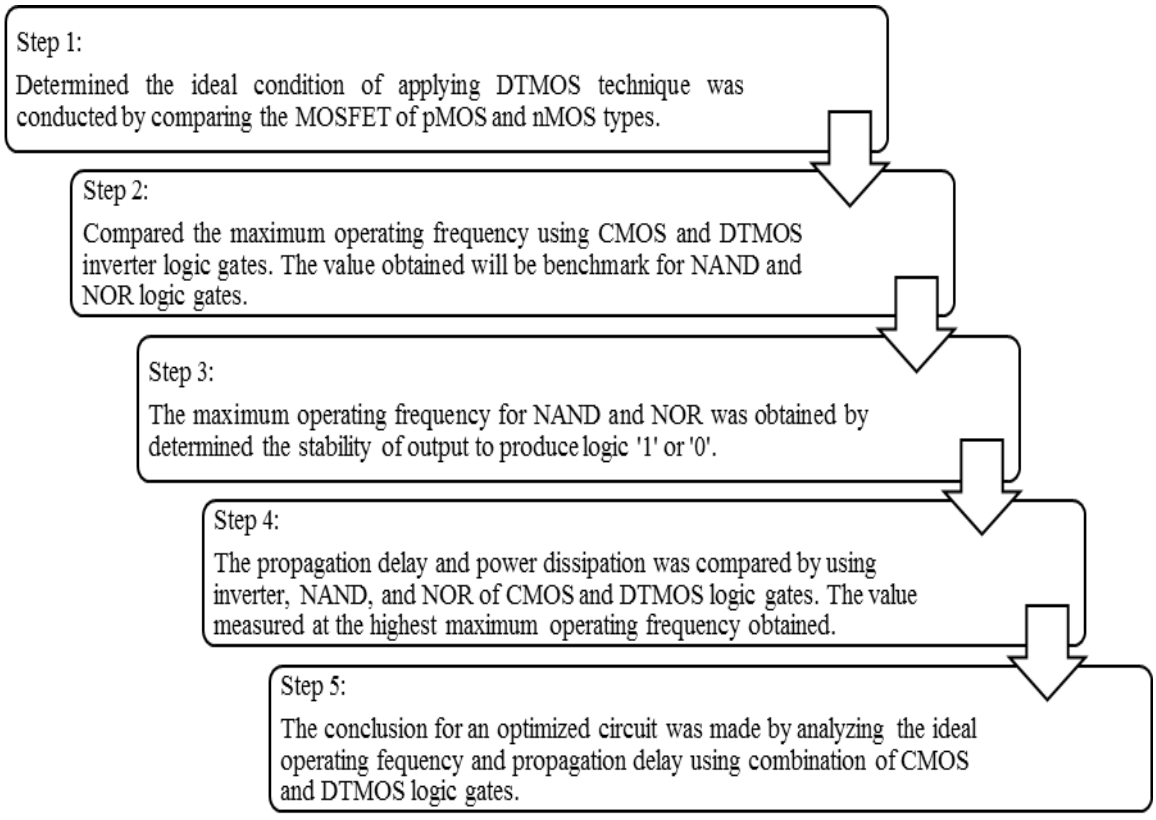


FIGURE 1. Methodology process diagram

This experiment were done using Mentor Graphic simulation with silicon 0.13µ size. Referring to Figure 1, at first the ideal condition of applying DTMOS technique was conducted by comparing the MOSFET of pMOS and nMOS types. The ideal condition of applying DTMOS technique was at pMOS transistor because if it was used on both transistors, the leakage current will be uncontrollable (Anand, 2002).

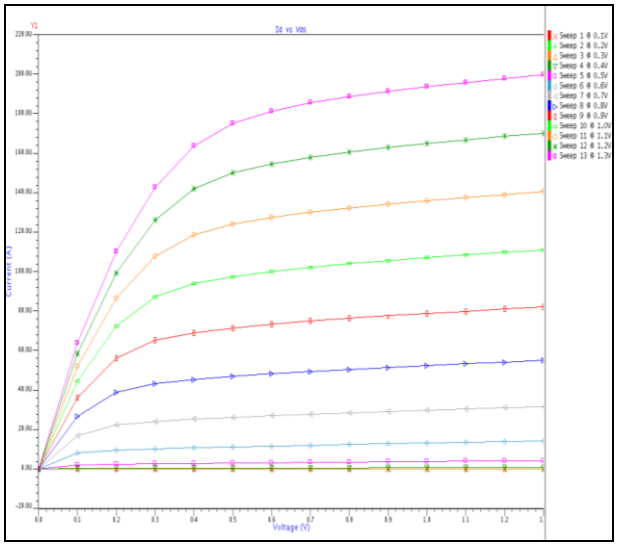
Next, the maximum operating frequency was compared using CMOS and DTMOS inverter logic gates. The reason is that because the inverter logic gates was the simplest in schematic diagram design and the most fundamental logic gates in IC design. The voltage input was set to 1V with all the properties of the transistors in Mentor Graphic was set to default. The result was recorded for the next experiment.

When the maximum operating frequency was obtained, the power dissipation and propagation delay was conducted on the basic logic gates which are inverter, NAND, and NOR. Furthermore, the NAND and NOR logic gates was expected to operate the maximum frequency at the same or lower than inverter logic gates. This is because NAND and NOR logic gates was more complicated than inverter logic gates with additional two transistors each one was pMOS and nMOS.

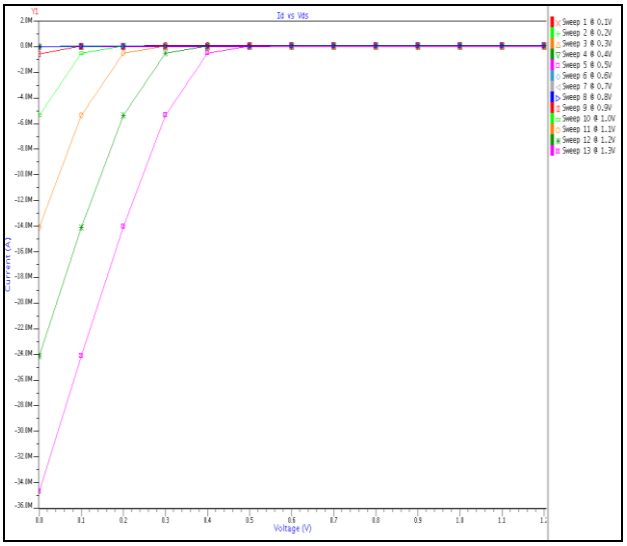
In order to determine the maximum operating frequency, the rise time of the transition logic '1' or '0' must not be half or more than the transition time. The reason is that when the rise time is at the middle of transition time, the logic output will appear as noise rather than logic '1' or '0'(Anand, 2002). The propagation delay was measured by comparing the rise or fall time between the input and the output of the logic circuits. Where else the power dissipation followed the formula of $P_d=I_dV_d$ where current (I_d) and voltage (V_d) are the average input measurements.

Lastly, the final experiment was to determine the best match of combination between CMOS and DTMOS logic circuit as a solution for optimizing circuit. The ideal condition was where the logic gates of CMOS and DTMOS operated at the same maximum frequency so that the output delay was not distorted. The power dissipation and propagation delay will not be considered because of the theoretically both types of logic gates received the same input voltage.

RESULTS AND DATA

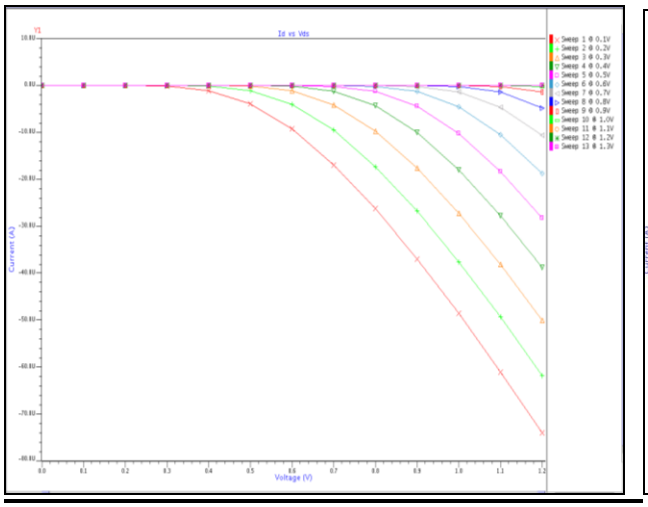


GRAPH 1. Drain current (I_d) vs Drain-source voltage (V_{ds}) for nMOS CMOS

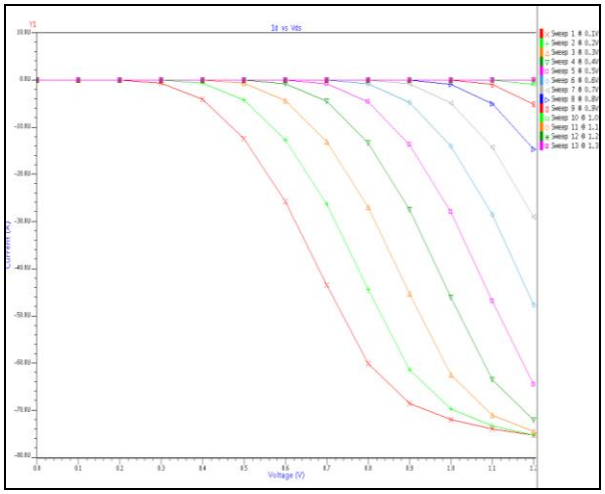


GRAPH 2. Drain current (I_d) vs Drain-source voltage (V_{ds}) for nMOS DTMOS

Based on figure 2 and figure 3, it showed early comparison between nMOS CMOS and nMOS DTMOS inverter logic gates. The voltage supplied was 1.2V with a sweep every 0.1V. For nMOS CMOS logic gates, it showed normal properties for conventional transistor but for nMOS DTMOS the threshold voltage (V_{th}) dropped significantly. According (Assaderaghi et al. 1997), the limit for threshold voltage was 0.4V for the tolerance of leakage current. However for nMOS transistors when the threshold voltage is high, the reverse-biased from bulk to source is also high. Then, when nMOS DTMOS transistors used more than 0.6V, it became forward-biased from bulk to source and forced the threshold voltage to drop significantly. The value for nMOS DTMOS transistors need to be set lower than 0.6V. Therefore, the nMOS transistors was not suitable for DTMOS technique in comparison with CMOS logic gates because the input voltage need to be more than 0.6V for equivalent results.



GRAPH 3. Drain current (I_d) vs Drain-source voltage (V_{ds}) for pMOS CMOS



GRAPH 4. Drain current (I_d) vs Drain-source voltage (V_{ds}) for pMOS DTMOS

Based on figure 4 and figure 5, it showed early comparison between pMOS CMOS and pMOS DTMOS inverter logic gates. The voltage supplied was 1.2V with a sweep every 0.1V. Unlike the result at nMOS transistors, the pMOS DTMOS transistor showed good comparison to pMOS CMOS transistor. The comparison between two graphs showed the DTMOS logic gates can produce threshold voltage much lower than CMOS logic gates at value 0.5V compared to 0.7V. This confirmed that DTMOS have the low voltage operation properties. On top of that the DTMOS technique at pMOS transistor can be operated at value more than 0.7V without leakage current problem. Thus, conclude that for comparison with CMOS logic gates the DTMOS logic gates applied its technique at pMOS transistors.

Inverter logic gate	**CMOS**	**DTMOS**
Propagation Delay (ps)	84.87	88.62
Max Operating Frequency (GHz)	5.0	5.0
Power Dissipation (µW)	23.22	7.93

TABLE 1. CMOS vs. DTMOS Inverter Logic Gates

NOR logic gate	**CMOS**	**DTMOS**
Propagation Delay (ps)	243.49	313.57
Max Operating Frequency (GHz)	2.0	2.0
Power Dissipation (µW)	10.70	7.23

TABLE 2. CMOS vs. DTMOS NAND Logic Gates

NAND logic gate	**CMOS**	**DTMOS**
Propagation Delay (ps)	154.83	285.55
Max Operating Frequency (GHz)	3.33	2.0
Power Dissipation (µW)	13.41	7.24

TABLE 3. CMOS vs. DTMOS NOR Logic Gates

As shown above, table 1, table 2, and table 3 showed the comparison value of CMOS and DTMOS in term of propagation delay, max operating frequency, and power dissipation of three types of logic gates which are inverter, NAND, and NOR. Each logic gates operate at their highest possible frequency when the data was recorded. The delay for the simulation was set to zero and with each fall time (t_f) and rise time (t_r) set to 25ps respectively. Other setting was remained at default value with no changes.

The first parameter which is maximum operating frequency was measured by observing the stability of the logic gates to performed good logic output either '1' or '0'. The observation was done by measuring the t_r to peak value must not more than or equal to half the time between t_r and t_f. This was because the logic will be considered as noise when the action mentioned occurred (Kaushik et al. 2001). Based on the three tables, inverter logic gates was the highest maximum operating frequency recorded. It became the benchmark for remaining two logic gates because it consists of only two transistors that allowed to achieve such high frequency. Where else, the other two logic gates, NAND and NOR consist of for transistors which theoretically can't overcome inverter operating frequency. The inverter and NOR of CMOS and DTMOS logic gates both can operate at the same frequency but NAND logic gates showed that CMOS can operate at much higher frequency than DTMOS. This is because of body effect at pMOS NAND logic gates required the transistor to have high input voltage when applying DTMOS technique in order to get same frequency result as CMOS logic gates.

Furthermore, all three logic gates showed comparison that CMOS had less propagation delay than DTMOS. This mean CMOS logic gates have much higher input to output ratio of logic processing time compared to DTMOS. The reason was because of the DTMOS technique that tied bulk to the input gate of transistors rather than tied bulk to the drain voltage (V_{dd}). The bulk of DTMOS logic gates have to wait for input signal before can operate compared to CMOS logic gates bulk that constantly charged with voltage from V_{dd}. For high calculation or logic operation was suitable to used CMOS logic gates because of its less delay time.

Although seems all parameter was a win for CMOS logic gates, the last parameter showed what DTMOS are made up from. The power dissipation showed all three types DTMOS logic gates have almost the same with less value compared to CMOS logic gates. With formula for finding power dissipation $P_d=I_dV_d$, where I_d was the current dissipate at the input and V_d was the input gate voltage that dissipate. As mentioned earlier, the properties of low threshold voltage for DTMOS logic gates enable it to produce low power dissipation compared to CMOS logic gates. This explained that DTMOS logic gates suitable for low power IC.

CONCLUSION

The experiment was conducted successfully using Mentor Graphic simulation of silicon at 0.13µ size. The results obtained was different from the expected situation. As we know, DTMOS logic gates showed lower power characteristic to win over CMOS logic gates. Eventually, DTMOS logic circuits failed to overcome CMOS logic gates on two parameters which are maximum operating frequency and propagation delay.

The maximum operating frequency of both showed that DTMOS was comparable to CMOS but in actual observation it was suggested that CMOS logic gates had the best stability compared to DTMOS logic gates. It was suggested a combination of an optimized circuit between CMOS and DTMOS can be done with in an IC the inverter and NOR logic gates using DTMOS technique. This was because the CMOS and DTMOS inverter and NOR logic gates can operate at the same maximum frequency. While NAND logic gates showed great gap in propagation delay and was not suitable for optimized circuit.

Lastly, with the advancement of today fabrication technology, there was a chance that DTMOS logic gates are comparable with CMOS logic gates at nano scale size. As the scaling factor becoming more small, DTMOS logic gates is the key for next generation of MOSFET to overcome CMOS problem at nano scale such as short channel effect. The experiment may be continued using more powerful simulation.

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